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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,706	07/24/2006	Takefumi Nishimuta	5000-5291	9357

85775 7590 07/22/2009

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EXAMINER	
BELOUSOV, ALEXANDER	
ART UNIT	PAPER NUMBER
2894	

NOTIFICATION DATE	DELIVERY MODE
07/22/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptopatentcommunication@lockelord.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,706	NISHIMUTA ET AL.	
	Examiner	Art Unit	
	ALEXANDER BELOUSOV	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6 and 9-19* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed on 04/27/2009. Currently, claims 1-3, 5-6 & 9-13 have been examined.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claim(s) 1-3, 5-6 & 9-13** is/are rejected under 35 U.S.C. 103(a) as being unpatentable over (US-2003/0102497) by Fried et al ("Fried") in view of (JP-8-264764) by Inoue (part of Applicant's IDS; therefore, it is not mentioned on the "Notice of References" and no translation is provided, since the Applicant was the one who provided it).

Regarding claim 1, Fried discloses in FIG. 7a-b and related text, **e.g.**, a MIS transistor, comprising:

a semiconductor substrate (200 in FIG. 2b; 202 & 206 are parts of it; also, see paragraph 41; it states that non-SOI device can be made and that layer 204 is ***not there*** as paragraph 41 makes clear; so, for the purpose of illustration, imagine that 204 is ***completely gone*** FIG. 7b and that 202, 204 & 206 is all 202) having a surface with a principal crystal plane comprising a projecting part (206 is "projecting part") formed directly from the surface of the semiconductor substrate (as it would be in non-SOI embodiment, as disclosed in paragraph 41) and at least one of a top surface and a side wall of the projecting part has a secondary crystal plane different from

the principal crystal plane (as far as "principal crystal plane" and a "secondary crystal plane" see Abstract and FIG. 7b; this is exactly what Fried discloses);

a gate insulator (208 & 210) formed on the semiconductor substrate including the projecting part in such a way that the gate insulator covers at least a portion of the semiconductor substrate, the top surface and the side wall of the projecting part (first of all, 208 & 210 directly touch all of the above, including 204 which would be 202 in non-SOI embodiment, as was made clear above, and thus meets the limitations; furthermore, this is not shown in the FIG. 7b since it is a SOI embodiment, but, the 210 or another oxide would ***inherently*** be under the entire gate 212, ***otherwise*** the gate would short to the semiconductor substrate and the device would not operate; this is an ***inherent*** feature; for the purposes of demonstrating a point, and not prior art, see FIG. 8 of US-5391506 by Tada; gate insulator 30 is everywhere under the gate electrode 32; again, this is an inherent feature of MIS/MOS transistors);

a gate electrode (212) formed on the gate insulator including the projecting part, said gate electrode being elongated in the direction of a gate length and in the direction of a gate width (see FIGs. 7a-b);

a plurality of channel regions formed at said top surface of said projecting part, at the surface of said side wall of said projecting part (see paragraph 51; this is where doping of the entire fin is done, before formation of gate electrode and before doping of the S/D; hence, this is where the doping of the channel region occurs; paragraph 51 states that "ion implantation may comprise ***an angled implant*** into exposed opposing vertical sidewalls 207 of semiconductor layer 206"; see FIG. 4b; "an angled implant into exposed opposing vertical sidewalls" would necessarily include implant of dopants into top left and top right corners of 206; hence, meeting

limitations of "said top surface" and "the surface of said side walls"; furthermore, as the Applicant is well aware, the ion implantation steps are followed by annealing steps, in order to repair the damage to crystal and to spread the dopants; hence, the dopants cover a lot more of "top surface" than only the top left and top right corners of fin 206), all under said gate insulator ("all under said gate insulator" is ***inherent***, as was explained above; otherwise the channel would short to the gate); and

a pair of diffusion regions (paragraph 57; "the S/D ***regions***… comprising the fin bodies") formed at said top surface of said projecting part, at the surface of said side wall of said projecting part (see paragraph 57; S/D are formed by doping "exposed portions of the fins" in FIG. 7b; hence, "top surface" and "the surface of said side wall" would receive dopants, meeting above limitations), all on both sides of the gate electrode in the direction of said gate length on the semiconductor substrate including the projecting part (inherent locations of S/D regions).

Fried does not explicitly state a plurality of channel regions formed ***at the surface of said at least a portion of said semiconductor substrate***; and a pair of diffusion regions formed ***at the surface of said semiconductor substrate***.

As has been made clear above, even though the Fried's default embodiment is on a SOI wafer, the non-SOI embodiment is disclosed in paragraph 41. However, Fried does not provide explicit teachings with regards to channel regions and S/D regions in a non-SOI case. Would those regions be also formed on the substrate itself? FIG. 7a (see the extent of the gate) would suggest that the answer should be "yes", but, no explicit teachings are provided. Therefore, a secondary reference is provided to teach the missing limitations.

Inoue discloses in FIG. 2 and related text, **e.g.**, a plurality of channel regions formed ***at the surface of said at least a portion of said semiconductor substrate*** (see FIG. 22(b); it shows channel directly under 5; FIG. 22(c) shows that there are a plurality of such regions); and a pair of diffusion regions formed ***at the surface of said semiconductor substrate*** (again, see FIG. 22(b); it shows the pair of diffusion regions (directly under 7 & 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Fried with a plurality of channel regions formed ***at the surface of said at least a portion of said semiconductor substrate***; and a pair of diffusion regions formed ***at the surface of said semiconductor substrate***, in order to efficiently use all the available semiconductor area (imagine FIG. 22 without the channels and a pair of diffusion regions being formed; that semiconductor area would not be used to increase the area of transistor, and therefore would be wasted).

Examiner's Note: please notice that the Inoue reference provides evidence for the various inherency statements made by the Examiner).

Regarding claim 2, Fried discloses in FIG. 7a-b and related text, **e.g.**, a channel width of a channel of the MIS transistor formed along with the gate insulator is defined by summation of each width of channels formed along with the gate insulator including the width and height of the projecting part (see FIG. 7b; the channel is exactly in the "projecting part"; and even though this is product-by-process limitation, the "channel" was "formed along with gate insulator", because until the gate insulator (and gate, and source, and drain) are formed, there was no channel).

Regarding claim 3, Fried discloses in FIG. 7a-b and related text, **e.g.**, the gate insulator continuously covers the top surface and the side wall of the projecting part (***inherent***: if the gate

insulator ***did not*** continuously cover the surface of the projecting part, the gate electrode would short to the projecting part or the substrate (as was made clear above) and the device would not be operational).

Regarding claim 5, Fried discloses in FIG. 7a-b and related text, **e.g.**, the MIS transistor (paragraph 2) comprising:

a semiconductor substrate (200 in FIG. 2b; 202 & 206 are parts of it; also, see paragraph 41; it states that non-SOI device can be made and that layer 204 is ***not there*** as paragraph 41 makes clear; so, for the purpose of illustration, just imagine that the line dividing 202 & 204 is gone in FIG. 7b and that it is all 202) having a surface with a principal crystal plane comprising a projecting part (206 is projection) formed directly from the surface of the semiconductor substrate (as it would be in non-SOI embodiment, as disclosed in paragraph 41) and at least one of a top surface and a side wall of the projecting part has a secondary crystal plane different from the principal crystal plane (as far as "principal crystal plane" and a "secondary crystal plane" see Abstract and FIG. 7b; this is exactly what Fried discloses);

a gate insulator (208 & 210) covering at least a portion of the semiconductor substrate, the top surface and the side wall of the projecting part (first of all, 208 & 210 directly touch all of the above, including 204 which would be 202 in non-SOI embodiment, as was made clear above, and thus meets the limitations; furthermore, this is not shown in the FIG. 7b since it is a SOI embodiment, but, the 210 or another oxide would ***inherently*** be under the entire gate 212, ***otherwise*** the gate would short to the semiconductor substrate and the device would not operate; this is an ***inherent*** feature; for the purposes of demonstrating a point, and not prior art, see FIG.

8 of US-5391506 by Tada; gate insulator 30 is everywhere under the gate electrode 32; again, this is an inherent feature of MIS/MOS transistors);

a gate electrode (212) formed on the gate insulator thereby the gate electrode is electrically insulated from the semiconductor substrate (as explained above and evidenced by Tada reference);

a plurality of channel regions formed at said top surface of said projecting part, at the surface of said side wall of said projecting part, all under said gate insulator (as explained with regards to claim 1); and

a pair of diffusion regions (paragraph 57; "the S/D **regions**… comprising the fin bodies") of the same conductivity type (inherent feature of S/D regions) formed at said top surface of said projecting part, at the surface of said side wall of said projecting part (as explained with regards to claim 1), all on both sides of the gate electrode on the semiconductor substrate (inherent location of S/D regions; 206 is part of the substrate, as was made clear above).

Fried does not explicitly state a plurality of channel regions formed ***at the surface of said at least a portion of said semiconductor substrate***; and a pair of diffusion regions formed ***at the surface of said semiconductor substrate***.

Inoue discloses in FIG. 2 and related text, **e.g.**, a plurality of channel regions formed ***at the surface of said at least a portion of said semiconductor substrate*** (see FIG. 22(b); it shows channel directly under 5; FIG. 22(c) shows that there are a plurality of such regions); and a pair of diffusion regions formed ***at the surface of said semiconductor substrate*** (again, see FIG. 22(b); it shows the pair of diffusion regions (directly under 7 & 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Fried with a plurality of channel regions formed ***at the surface of said at least a portion of said semiconductor substrate***; and a pair of diffusion regions formed ***at the surface of said semiconductor substrate***, in order to efficiently use all the available semiconductor area (imagine FIG. 22 without the channels and a pair of diffusion regions being formed; that semiconductor area would not be used to increase the area of transistor, and therefore would be wasted).

Regarding claim 6, Fried discloses in FIG. 7a-b and related text, **e.g.**, the gate insulator continuously covers the top surface and the side wall of the projecting part (***inherent***: if the gate insulator (208 & 210) did not continuously cover the semiconductor, the gate electrode would short to the semiconductor, and the device would not be operational, as was made clear above, and evidenced by Tada reference).

Regarding claims 9 & 10, Fried discloses in FIG. 7a-b and related text, **e.g.**, wherein the MIS transistor is a signal transistor (***inherent***: transistors can be "on" or "off", hence at least two different signals).

Regarding claims 11 & 12, Fried discloses in FIG. 7a-b and related text, **e.g.**, the semiconductor substrate is a silicon substrate (paragraph 44: "***any*** semiconductor material") and the hydrogen content at an interface of the silicon substrate and the gate insulator is 10.sup.11/cm.sup.2 or less in units of surface density (Fried does not disclose ***any*** usage of hydrogen, hence the hydrogen content is "zero").

Regarding the process limitations recited in claims 11 & 12 ("the gate insulator ***is formed by*** exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to

remove hydrogen"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claim 13, Fried discloses in FIG. 7a-b and related text, **e.g.**, the semiconductor substrate is a silicon substrate (paragraph 44: "***any*** semiconductor material"), and each of the principal crystal plane and the crystal planes of the top surface and the side wall of the projecting part are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane (see paragraph 40).

Response to Arguments

1. Applicant's arguments with respect to above claims have been considered but are moot in view of the new ground(s) of rejection.

2. The rest of Applicant's Arguments are moot in light of new grounds for rejection.

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office

action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Belousov whose telephone number is 571-270-3209. The examiner can normally be reached on Monday - Thursday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander Belousov/
Examiner, Art Unit 2894
07/17/2009

/Bradley K Smith/
Primary Examiner, Art Unit 2894